REMARKS

In the present Office Action, claims 1 - 17 were pending before the Office. Of these, claims 1, 7, 8, 16, and 17 were the only independent claims.

Claims 10 - 15 and 17 were rejected under 35 U.S.C. § 112, first paragraph. Claims 1 - 3, 5 - 9, and 16 were rejected under 35 U.S.C. § 102(e).

No claims have been hereby added, amended, canceled, or withdrawn.

A. THE CLAIM REJECTION UNDER 35 U.S.C. § 112, FIRST PARAGRAPH, IS CLEARLY NOT PROPER AND IS CLEARLY WITHOUT BASIS AS PAGES 5 - 7 OF THE SPECIFICATION CLEARLY ENABLE CLAIMS 10 - 15 AND 17

Claims 10 - 15 and 17 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. For at least the reasons set forth herein, Applicants respectfully traverse this rejection.

Claims 10 and 17 recite, inter alia:

> determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state.

Specifically, the Examiner contends that

> [W]hen only the select signal E1 is in the first logic state (in logic state high as described in the specification), and the others are in a second logic state (in logic state low as described in the specification). [sic] That causes NAND gate 206a and the latches outputting a logic state low output; [sic] which will cause other select signals E2-E4 passed through other NAND gates and latches because all of select signals (C1-C4 of NAND gates 206b-206d) as described in the

> disclosure (page 6, line 14 thorugh page 7, line 1). [sic]

Applicants respectfully submit that the rejection is clearly not proper and is without basis. Specifically, Applicants respectfully submit that (1) the above contention is not comprehendible, and (2) the specification as originally filed provides more than sufficient support to enable one of ordinary skill in the art to "determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state."

Applicants respectfully submit that the above contention is not comprehensible. For this reason alone, Applicants respectfully submit that the rejection clearly fails to establish a prima facie case of non-enablement.

Moreover, Applicants respectfully maintain that page 6, line 14 through page 7, line 15, of the specification provide more than sufficient support to enable one of ordinary skill in the art to "determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state." This is especially true in light of page 5, line 31 through page 6, line 13 (e.g., "With reference to FIG. 2, the SOSD circuit 114 comprises a plurality of sub-circuits 202a-d each adapted to generate a different one of the synchronized select signals C1-C4 from the unsynchronized select signals E1-E4.")

Applicants respectfully submit that the rejection is clearly not proper and is clearly without basis. Accordingly, favorable reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, first paragraph, are respectfully requested.

B. THE CLAIM REJECTION UNDER 35 U.S.C. § 102 IS CLEARLY NOT PROPER AND IS CLEARLY WITHOUT BASIS AS THE CITED REFERENCE DOES NOT DISCLOSE PREVENTING A FIRST SELECT SIGNAL IN A FIRST LOGIC

STATE FROM BEING PROVIDED TO A MULTIPLEXER UNTIL ALL OTHER SELECT SIGNALS ARE IN A SECOND LOGIC STATE.

Claims 1 - 3, 5 - 9, and 16 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,600,355 to Nguyen [hereinafter *Nguyen*]. For at least the reasons set forth herein, Applicants respectfully traverse this rejection.

Claim 1 recites, inter alia:

> preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state.

Claim 7 recites, inter alia:

> preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state[.]

Claim 8 recites, inter alia:

> selection circuitry coupled to the multiplexer and adapted to prevent a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state.

Claim 16 recites, inter alia:

> prevent a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state[.]

Applicants respectfully submit that the rejection is clearly not proper and is without basis. Specifically, Applicants respectfully submit that the sole reference *Nguyen*

does not disclose at least the above features, for at least the reasons herein. Accordingly, a prima facie case of obviousness has not been established.

The Examiner contends that

> As discussed above, for example, Nguyen clearly teaches a multiplexer system (as shown in FIG. 2) comprising a selection circuitry (201) which only provides one of the select signals, i.e., the select signal S270, is (sic) in the first logic state (High) while other select signals, i.e., the select signals S0, S90 and S180, are in the second logic state (Low).

The above quotation offers absolutely no citation to *Nguyen* for even mentioning a first logic state or a second logic state. In fact, an electronic search of *Nguyen* reveals that *Nguyen* does not contain the phrases "first logic state," "second logic state," "low state," or "high state." Rather, *Nguyen* discloses, at most, select signals output by a state machine and clock signals being provided to a multiplexer.

Applicant respectfully submits that the rejection is clearly not proper and is without basis. Accordingly, favorable reconsideration and withdrawal of the rejection under 35 U.S.C. § 102 are respectfully requested.

C. CONCLUSION

Since Applicants assert that all the independent claims are in condition for allowance and all remaining claims properly depend from the independent claims, Applicants assert that all claims are allowable.

Applicants do not believe a request for extension of time is required but if it is, please accept this paragraph as a request for an extension of time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicants do not believe any additional fees are due regarding

this amendment. However, if any additional fees are required, please charge Deposit Account No. 04-1696.

Respectfully Submitted,

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